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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,318	10/24/2001	David Patrick Magee	TI-32985	2991

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EXAMINER	
FLANAGAN, KRISTA M	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,318	MAGEE, DAVID PATRICK	
	Examiner	Art Unit	
	Krista M. Flanagan	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-19 and 22-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-29* is/are allowed.

6)☒ Claim(s) *1, 6, 7, 8, 12, 13 and 15-19* is/are rejected.

7)☐ Claim(s) *2-5,11 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

EXAMINER'S ANSWER

Drawings

1. In view of the amendment filed on 09 May 2005, the Examiner withdraws objections to the drawings from the previous Office Action.

Specification

2. In view of the amendment filed on 09 May 2005, the Examiner withdraws objections to the specification from the previous Office Action.

Claim Objections

3. Claim 11 is objected to because of the following informalities: Claim 11 shows dependency from claim 10, which has been canceled. In the remarks, applicant states that claim 11 has dependency from claim 8. Appropriate correction is required.

Response to Arguments

4. Applicant's arguments filed on 2005 have been fully considered but they are not persuasive.

5. The Applicant contends, "Regarding claim 1, the Examiner has stated that Nagayasu discloses 'a channel estimator component (See figure 1) operative to process a data signal to form a current channel impulse response (See figure 1, blocks 12 and 14) and a channel estimate;' (emphasis added). Applicants respectfully disagree. Blocks 12 and 14 are channel impulse response (CIR) estimators and they only estimate it at different positions in a received burst (See col. 8, lines 30-43). In contrast, claim 1 recites a channel estimator component operative to process a data signal to form a current channel impulse response **and** a channel

estimate. Blocks 12 and 14 of Nagayasu et al. do not provide a channel estimate as recited in claim 1."

6. The Examiner disagrees and asserts, that, Nagayasu does disclose a channel estimator that provides a channel estimate. It is well known in the art that a channel estimate is the same as a channel impulse response. Therefore, Nagayasu does disclose providing a channel estimate. The Examiner suggests that the applicant claim the channel estimate as described in the specification. The claims omit the steps recited in the specification where the channel estimator zero pads and performs FFT on the channel impulse response to find the channel estimate. The claim just states that the channel estimator component is operative to process a data signal to form a channel impulse response and a channel estimate. There is no recitation in the claim on how this channel estimate is found to make this clear as a separate product from the channel impulse response.

7. The Applicant contends, "Further, the Examiner has stated that Nagayasu et al. describe 'an offset phasor determiner (See figure 1, block 15 and column 8, lines 45-50) that determines an offset phasor as a function of the current channel impulse response and a previous channel impulse response' (emphasis added). Applicant respectfully disagree and point to the Examiner that Nagayasu et el. describe block 15 as a phase deviation circuit that estimates values at two different positions determined by channel impulse response estimating circuits 12 and 14. According to Nagayasu et al., these circuits estimate channel impulse response at two different positions within the same burst in a corrected received signal (see col. 8, lines 30-34 for unit 12; and col. 8, lines 38-43 for unit 14). In contrast, claim 1 recites an offset phasor determiner that determines an offset phasor as a function of the current channel impulse response and a previous

channel impulse response. Thus, Nagayasu et al. does not teach an offset phasor as a function of the current channel impulse response and a previous channel impulse response as recited in claim 1. Accordingly, claim 1 is patentably distinguishable from Nagayasu et al.

8. The Examiner disagrees and asserts, that, Nagayasu does disclose a channel estimate or channel impulse response based on two separate responses as is shown in the phase deviation detection circuit and corresponding text in column 8, lines 45-50 of the reference. A first channel impulse response is estimated at time M1 and a second response is estimated at time M2 and a phase deviation is computed.

9. The Applicant contends, "Applicants respectfully point to the Examiner that first, Nagayasu et al. is directed to and describes a receiver with a frequency offset correcting function (see col. 3, line 62 - col. 4, line 3) The frequency offset correcting circuit 11 depends on a frequency offset estimated value $\Delta\acute{\omega}_m$ received from the averaging circuit 16. If a phase corrector is used in place of the frequency corrector as the Examiner has asserted, then the entire circuit of Nagayasu et el. will have to be changed because a phase corrector will need different offset from the averagor because an ordinary person skilled in the art will not just replace a frequency corrector with phase corrector. Further, the functions of the CIR estimating circuits have to be modified, furthermore, the equalizer needs to be adjusted to respond to the phase corrected input rather than frequency corrected signal. Similarly, rest of the functions of the circuit will have to be modified to convert the frequency offset correcting function to a phase offset correcting function as the Examiner has asserted. This will basically change the entire circuit of Nagayasu et al. 'the proposed modification cannot render the prior art unsatisfactory for its intended purpose.' See MPEP 92143.01."

10. The Examiner disagrees and asserts, that, the frequency offset corrector of Nagayasu et al. could be replaced with a phase offset corrector. The frequency offset corrector uses the frequency offset estimated value, which is computed from the averaging circuit, which uses the phase deviation from the phase deviation detecting circuit. The phase offset is given to the averaging circuit and used to produce the frequency offset estimated value. In correcting the frequency offset, the phase offset is corrected also. Therefore, the frequency offset corrector the frequency offset corrector is also performing phase offset correction. The functions of the rest of the circuit would not need to be modified to respond to the phase corrected input because the input they respond to is just that as well as a frequency corrected input.

Claim Rejections - 35 USC § 112

11. In view of the amendment filed on 09 May 2005, the Examiner withdraws 112 rejections from the previous Office Action.

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps in both claims are: the channel estimator zero padding and performing FFT on the channel impulse response to find the channel estimate as stated on page 6, lines 20-22 of the applicant's specification. The claim just states that the channel estimator component is operative to process a data signal to form a channel impulse response and a channel estimate. There is no recitation in the claim on how this channel estimate is found to make this clear as a separate product from the channel impulse response.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1, 6, 7, 8, 12, 13 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagayasu et al., US Patent No. 6,347,126.

16. Regarding claim 1, Nagayasu discloses a receiver system comprising: a channel estimator component (See figure 1) operative to process a data signal to form a current channel impulse response (See figure 1, blocks 12 and 14) and a channel estimate; and an offset phasor determiner (See figure 1, block 15 and column 8, lines 45-50) that determines an offset phasor as a function of the current channel impulse response and a previous channel impulse response; and a frequency offset corrector (See figure 1, block 11) that corrects the current channel impulse response by the offset phasor and provides a phase corrected channel impulse response to the channel estimator, such that the channel estimator determines a corrected channel estimate (See figure 1, blocks 11 and 13). Nagayasu fails to disclose a phase offset corrector that provides a phase corrected channel impulse response to the channel estimator, such that the channel estimator determines a corrected channel estimate. However, he discloses a frequency offset corrector that provides a phase corrected channel impulse response to the channel estimator, such that the channel estimator determines a corrected channel estimate. It would be obvious to one of ordinary skill in the art to use a phase corrector in place of a frequency corrector. One could be motivated to do this since phase and frequency have a linear relationship.

17. Regarding claim 6, which inherits all of the limitations from claim 1, Nagayasu discloses a system wherein the channel estimate is at least partly formed from the phase corrected channel impulse response (See figure 1, blocks 12 and 14 and column 8, lines 27-38).

18. Regarding claim 7, which inherits all of the limitations from claim 1, Nagayasu discloses a system wherein the channel estimator determines an average channel impulse response (See figure 1, block 16 and column 8, lines 50-54).

19. Regarding claim 8, Nagayasu discloses a signal processing system for use in a receiver, the system comprising: a channel estimator (See figure 1) that receives a digital signal and produces a current channel impulse response, an average channel impulse response and a channel estimate; an offset phasor determiner (See figure 1, block 15 and column 8, lines 45-50) that determines an offset phasor, the offset phasor being at least partly a function of the current channel impulse response (See figure 1, block 14); and a frequency offset corrector (See figure 1, block 11) that corrects the current channel impulse response by the phase offset using the offset phasor and provides a frequency corrected channel impulse response. Nagayasu fails to disclose a phase offset corrector that corrects the current channel impulse response by the phase offset using the offset phasor and provides a frequency corrected channel impulse response. He discloses a frequency offset corrector that corrects the current channel impulse response by the phase offset using the offset phasor and provides a frequency corrected channel impulse response. It would be obvious to one of ordinary skill in the art to use a phase corrector in place of a frequency corrector. One could be motivated to do this since phase and frequency have a linear relationship.

20. Regarding claim 12, Nagayasu discloses a system for correcting a current channel impulse response, the system comprising: a component that receives a digital signal and produces a current channel impulse response (See figure 1, blocks 11, 12 and 14); an offset phasor determiner (See figure 1, block 15) that provides an offset vector that is a function of the current channel impulse response and a previous channel impulse response, the offset phasor determiner iteratively computes the sine and cosine of the phase offset from the offset vector (See column 7, lines 13-24); and a phase offset corrector (See figure1, block 11) that forms a phase corrected channel impulse response from the current channel impulse response and the offset phasor. Nagayasu does not expressly disclose performing an IFFT on the data bursts to obtain a channel impulse response or an FFT to transform the phase corrected channel impulse response into a portion of a channel estimate. However, it would be apparent to one of ordinary skill in the art that a signal can be represented as a function of time *t* or as a function of frequency *f*. One would be motivated to switch between the two representations by applying the fast Fourier transform or inverse fast Fourier transform.

21. Regarding claim 13, which inherits all of the limitations of claim 12, Nagayasu discloses a system wherein the offset vector is formed as a product of the previous channel impulse response and the complex conjugate of the current channel impulse response (See column 7, lines 13-24).

22. Regarding claim 15, Nagayasu discloses a system for determining a phase corrected channel impulse response, the system comprising: a comparator (See block 14 and column 7, lines 13-24) that computes an offset vector as a function of a current channel impulse response and a second channel impulse response, the offset vector representing a phase offset of the

current channel impulse response with respect to the second channel impulse response; a vector analyzer (See block 15) that computes an offset phasor as a function of the offset vector, the offset phasor having an imaginary component corresponding to the sine of the phase offset and a real component corresponding to the cosine of the phase offset; and a frequency offset corrector (See block 11, where the frequency corrector of Nagayasu has a linear relationship with a phase corrector of the current application.) that computes a corrected channel impulse response using the offset phasor.

23. Regarding claim 16, which inherits all of the limitations of claim 15, Nagayasu discloses a system wherein the second channel impulse response is one of an average channel impulse response and a previous channel impulse response (See figure 1, block 16).

24. Regarding claim 17, which inherits all of the limitations of claim 15, Nagayasu discloses a system wherein the comparator computes the offset vector as a product of the second channel impulse response and a complex conjugate of the current channel impulse response (See column 7, lines 13-24).

25. Regarding claim 18, which inherits all of the limitations of claim 15, Nagayasu discloses a system wherein the offset phasor being computed without computing the angle of the offset vector (See figure 1, block 15 and column 8, lines 45-50 where there is no mention of computing a start angle).

26. Regarding claim 19, which inherits all of the limitations of claim 15, Nagayasu discloses a system wherein the phase offset corrector corrects the current channel impulse response by the phase offset using the offset phasor (See figure 1, block 11).

Allowable Subject Matter

27. Claims 22-29 are allowed.

28. Claims 2-5, and 14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

29. Regarding claim 22, subject matter, allowable over prior art, is highlighted. "A method for determining an offset phasor comprising: providing a first channel impulse response and a second channel impulse response forming an offset vector as a function of the first channel impulse response and the second channel impulse response, where the offset vector has an x coordinate and a y coordinate; **initializing a first vector having an x component and a y component with a constant value for the x component and with a zero value for the y component; initializing a second vector having an x component and a y component with the x and y coordinates of the offset vector, respectively', incrementally rotating the first vector until the y component of the second vector is about zero; concurrent to rotating the first vector, incrementally rotating the second vector in an opposite direction of the first vector until the y component of the second vector is about zero; and providing an offset phasor being final components of a last iteration of the first vector**, the x component being the cosine of the angle formed by the offset vector and the y component being the sine of the angle formed by the offset vector."

Conclusion

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Krista M. Flanagan whose telephone number is (571) 272-2203. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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